AMENDMENTS TO THE CLAIMS

Claim 1 (Currently amended): A system comprising:

a memory having linearly addressable storage units to store video data; and

a programmable video direct memory access (VDMA) controller to access the storage units of the memory in response to a command specifying a multidimensional block of video data and fetch the multidimensional block of video data from multiple non-contiguous rows of the memory in response to the command.

Claim 2 (Original): The system of claim 1, wherein the command specifies a number of rows and a number of columns for the block of video data.

Claim 3 (Original): The system of claim 1, wherein the command specifies a jump parameter indicating a number of storage units between each row of the video block.

Claim 4 (Original): The system of claim 1, wherein in response to the command, the VDMA controller copies the video data from the memory to a destination memory.

Claim 5 (Original): The system of claim 4, wherein the command specifies a starting address of the video block within the memory, and a starting address within the destination memory.

Claim 6 (Canceled).

Claim 7 (Original): The system of claim 1, further comprising:

a processor to issue commands to the VDMA controller via a first bus; and

a digital signal processor to issue commands to the VDMA controller via a second bus.

Claim 8 (Original): The system of claim 1, further comprising a motion estimation unit having an internal memory and a differential calculator to calculate a distortion metric between blocks of

video data, wherein the VDMA controller copies blocks of video data from the memory to the internal cache of the motion estimation unit in response to the command.

Claim 9 (Currently amended): A method comprising:

receiving a direct memory access (DMA) command from a processor to transfer a multidimensional block of video data;

generating a set of source addresses and a set of destination addresses for the multidimensional block of video data in response to the command, wherein the set of source addresses correspond to multiple non-contiguous rows of a source memory; and

copying video data from ~~a~~ the source memory to a destination memory according to the source addresses and destination addresses in response to the command.

Claim 10 (Original): The method of claim 9, wherein the source memory and the destination memory each have linearly addressable storage units.

Claim 11 (Original): The method of claim 9, wherein the command specifies a number of rows and a number of columns for the block of video data, and wherein generating a set of addresses comprises calculating the source addresses and destination addresses as a function of the number of rows and the number of columns.

Claim 12 (Original): The method of claim 9, wherein the command specifies a jump parameter indicating a number of addresses between each row of the video block, and wherein generating a set of addresses comprises calculating the source addresses and destination addresses as a function of the jump parameter.

Claim 13 (Original): The method of claim 9, wherein the command specifies a starting source address of the video block within the source memory, and a starting destination address within the destination memory.

Claim 14 (Original): The method of claim 9, wherein copying video data comprises fetching an entire block of video data having multiple rows in response to the command.

Claim 15 (Original): The method of claim 9, wherein receiving the command comprises receiving the command via a first bus, the method further comprising receiving a second command from a digital signal processor via a second bus.

Claim 16 (Original): The method of claim 9, wherein copying video data comprises copying the video data to an internal cache of a motion estimation unit in response to the command.

Claim 17 (Currently amended): A device comprising:

a first memory to store a candidate video block to be encoded;

a second memory to store a set of video data blocks from which to encoded the candidate video block; ~~and~~

a differential calculator to calculate differential metrics between the candidate video block and the set of video blocks; and

a programmable video direct memory access (VDMA) controller to copy the candidate video block and the set of video blocks from a video memory to the first memory and the second memory, respectively, wherein the VDMA controller copies the set of blocks to the second memory in response to a single direct memory access (DMA) command specifying a multidimensional search space of video data stored within the video memory in multiple non-contiguous rows.

Claim 18 (Original): The device of claim 17, wherein the set of video data blocks stored by the second memory comprises a complete video data frame.

Claim 19 (Currently amended): The device of claim 17, wherein the differential calculator include address generation logic to read the candidate video block from the first memory ~~cache~~ and one or more video blocks of the set of video blocks from the second memory ~~cache~~.

Claim 20 (Currently amended): The device of claim 19, wherein the differential calculator reads the candidate video block from the first memory ~~cache~~ and one or more video blocks of the set of video blocks from the second memory ~~cache~~ in parallel.

Claim 21 (Cancel)

Claim 22 (Cancel)

Claim 23 (Original): The device of claim 22, wherein the command specifies a number of rows and a number of columns for the search space of video data.

Claim 24 (Original): The device of claim 21, wherein the video memory includes a plurality of linearly addressable storage units to store video data.

Claim 25 (Currently amended): The device of claim 21, wherein the command specifies a jump parameter indicating a number of storage units between each row of the search space. ~~video block.~~

Claim 26 (Currently amended): The device of claim 21, wherein the command specifies a starting source address of the search space ~~video block~~ within the video memory, and a starting destination address within the second memory. ~~cache.~~

Claim 27 (Cancel)

Claim 28 (Original): The device of claim 21, further comprising:

a processor to issue commands to the VDMA controller via a first bus; and

a digital signal processor (DSP) to issue commands to the VDMA controller via a second bus.

Claim 29 (Original): The device of claim 17, wherein the differential calculator calculates the differential metrics in response to search commands, and wherein each search command specifies a multidimensional region of video data stored within the second memory.

Claim 30 (Original): The device of claim 29, further comprising a command buffer to store the search commands and deliver the search commands to the differential calculator.

Claim 31 (Currently amended): A device comprising:

means for receiving a direct memory access (DMA) command from a processor to transfer a multidimensional block of video data;

means for generating a set of source addresses and a set of destination addresses for the multidimensional block of video data in response to the command, wherein the set of source address correspond to multiple non-contiguous rows of a source memory; and

means for copying video data from the ~~a~~ source memory to a destination memory according to the source addresses and destination addresses.

Claim 32 (Original): The device of claim 31, wherein the source memory and the destination memory each have linearly addressable storage units.

Claim 33 (Original): The device of claim 31, wherein the command specifies a number of rows and a number of columns for the block of video data, and wherein the generating means comprises means for calculating the source addresses and destination addresses as a function of the number of rows and the number of columns.

Claim 34 (Original): The device of claim 31, wherein the command specifies a jump parameter indicating a number of addresses between each row of the video block, and wherein the generating means comprises means for calculating the source addresses and destination addresses as a function of the jump parameter.

Claim 35 (Original): The device of claim 31, wherein the command specifies a starting source address of the video block within the source memory, and a starting destination address within the destination memory.

Claim 36 (Cancel)

Claim 37 (Original): The device of claim **31**, wherein the receiving means receives the command via a first bus and a second command from a digital signal processor via a second bus.

Claim 38 (Original): The device of claim **31**, wherein the copying means comprises means for copying the video data to an internal cache of a motion estimation unit in response to the command.